IOP Conf. Series: Journal of Physics: Conf. Series 993 (2018) 012010

Optimization of conditions for thermal smoothing GaAs surfaces

I O Akhundov^{1,2}, D M Kazantsev^{1,2}, A S Kozhuhov¹ and V L Alperovich^{1,2}

¹ Rzhanov Institute of Semiconductor Physics, 630090 Novosibirsk, Russia ² Novosibirsk State University, 630090 Novosibirsk, Russia

E-mail: akhundov@isp.nsc.ru

Abstract. GaAs thermal smoothing by annealing in conditions which are close to equilibrium between the surface and vapors of As and Ga was earlier proved to be effective for the step-terraced surface formation on epi-ready substrates with a small root-mean-square roughness ($R_q \le 0.15$ nm). In the present study, this technique is further developed in order to reduce the annealing duration and to smooth GaAs samples with a larger initial roughness. To this end, we proposed a two-stage anneal with the first high-temperature stage aimed at smoothing "coarse" relief features and the second stage focused on "fine" smoothing at a lower temperature. The optimal temperatures and durations of two-stage annealing are found by Monte Carlo simulations and adjusted after experimentation. It is proved that the temperature and duration of the first high-temperature stage are restricted by the surface roughening, which occurs due to deviations from equilibrium conditions.

1. Introduction

Atomically flat semiconductor surfaces are needed for fundamental surface science, fabrication of nanoscale structures and device applications. Smooth surfaces with a small root-mean-square (rms) roughness (comparable to or even smaller than inter-atomic distances) can be obtained by chemomechanical polishing (CMP) [1]. However, a surface prepared by CMP is disordered on a microscopic scale due to the mechanical impact during polishing. Annealing at elevated temperatures can effectively reduce this disorder and yield regular step-terraced surfaces with atomically flat terraces separated by steps of monatomic height. Almost perfect step-terraced silicon surfaces are obtained by annealing in vacuum [2,3,4]. For III-V semiconductors, the application of vacuum annealing is hindered by the evaporation of a more volatile V component. To overcome this difficulty and obtain step-terraced GaAs surfaces, annealing in MBE or MOCVD setups under As-contained vapors was used in papers [5,6]. A more efficient and cost-effective technique for GaAs smoothing was proposed in [7]. This technique consists of annealing GaAs substrates in a quartz tube of a liquid phase epitaxy (LPE) setup. The conditions close to equilibrium between the surface and vapors of As and Ga were provided by the presence of a saturated Ga-As melt. This technique proved to be effective for the GaAs step-terraced surface formation on epi-ready substrates with a relatively small root-mean-square roughness ($R_a \le 0.15$ nm). For such substrates, the step-terraced morphology was formed during about one-hour anneals in the temperature range of 600°C-650°C. The full length of monatomic steps was used for the quantitative characterization of the step-terraced morphology formation. The experimental kinetics of the step length was compared to Monte Carlo simulations within the Kossel crystal model

Content from this work may be used under the terms of the Creative Commons Attribution 3.0 licence. Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI. Published under licence by IOP Publishing Ltd 1