

Growth and characterization of $\text{CaF}_2/\text{Ge}/\text{CaF}_2/\text{Si}(111)$ quantum dots for resonant tunneling diodes operating at room temperature

A. I. Yakimov,^{a)} A. S. Derjabin, L. V. Sokolov, O. P. Pchelyakov, and
A. V. Dvurechenskii

*Institute of Semiconductor Physics, Siberian Branch of the Russian Academy of Sciences,
630090 Novosibirsk, Russia*

M. M. Moiseeva and N. S. Sokolov

*A. F. Ioffe Physical-Technical Institute, Russian Academy of Sciences, Politekhnicheskaya 26,
194021 St. Petersburg, Russia*

(Received 8 January 2002; accepted for publication 21 May 2002)

Resonant tunneling diodes were implemented on Ge quantum dots fabricated using Stranski–Krastanov growth mode on CaF_2 matrix, lattice matched to Si(111) substrates. The negative differential conductance and conductance oscillations due to hole resonant tunneling through the zero-dimensional states of Ge quantum dots are clearly observed at room temperature. From the period of conductance oscillations, the energy separations between the states of the quantum dots with different sizes are estimated to be 40–50 meV (i.e., $>kT=26$ meV at $T=300$ K). © 2002 American Institute of Physics. [DOI: 10.1063/1.1494465]

Three-dimensional quantum confinement in a semiconductor quantum dot (QD) leads to the formation of zero-dimensional (0D) states with discrete energies. The interplay between resonant tunneling through 0D states and single-electron charging effects underlies operation of single electron tunneling (SET) devices. Development of silicon-compatible nanoelectronics has attracted considerable interest in recent years. For future application of SET diodes, it is necessary to rise the operation temperature of the devices up to 300 K. To satisfy this condition, the size of QDs has to be smaller than 10 nm. This requirement considerably restricts the possibility of using the lithographic processes for fabrication ultrasmall QDs. In this way the self-assembled quantum dots, which are formed without additional lithography procedure and whose diameter can be achieved as small as 10 nm are more advantageous and hence more relevant for application in SET devices operating at room temperature.

To date most work in the field of silicon-compatible resonant tunneling diodes is concentrated on arrays of Si nanocrystallites (nc-Si) embedded in a double-barrier structure with ultrathin SiO_2 barriers. In these previous samples, $\text{SiO}_2/\text{Si}/\text{SiO}_2$ structures were produced either by simultaneous crystallization and oxidation of amorphous silicon^{1–3} or by decomposition of SiH_4 in various combinations.^{4–7} Recently, single-electron tunneling effects have also been observed in phosphosilicate glass films containing nc-Si⁸ and in silicon nanopillars with silicon nitride tunneling barriers.⁹ Arrays of Ge self-assembled QDs embedded in silicon represent another attractive type of SET devices.^{10,11} However, until now, the resonant tunneling effects in Ge/Si QDs were observed at only $T < 200$ K.^{10–12} The reason is a relatively narrow band gap of Si (~ 1 eV) with respect to insulators (~ 10 eV), which makes thermoelectronic emission over Si barriers to be effective at high temperatures. In this work, we

report on the fabrication and electrical characteristics of tunneling devices made up of Ge nanoclusters embedded in CaF_2 thin films and grown on a Si(111) substrate. One of the purposes of employing calcium fluoride as tunneling barriers instead of silicon is the much higher barrier height (the band gap of CaF_2 is 12 eV) that provide the potential to operate at higher temperatures. Moreover, the CaF_2 –Si pair has a small lattice mismatch of about 0.6% at room temperature, and the fluorite-like structure of CaF_2 is similar to the diamond-like structure of Si. These features grow the crystalline pseudomorphic insulator films of CaF_2 on Si(111) surfaces instead of SiO_2 films which are always amorphous and have a number of intrinsic defects. The current–voltage measurement of the devices displays negative differential conductance and conductance oscillations at room temperature.

For resonant tunneling experiments, a layer of Ge quantum dots is embedded between two 2-nm-thick CaF_2 tunneling barriers on top of a $0.005 \Omega \text{ cm } p^+$ -Si(111) substrate, which acts as an ohmic back side contact. The top contact is formed by deposition of a fully relaxed 20-nm-thick p^+ -Ge layer (Fig. 1). The growth details are following. The samples were grown in UHV MBE system equipped with RHEED system with a 40 kV electron gun. After RCA chemical

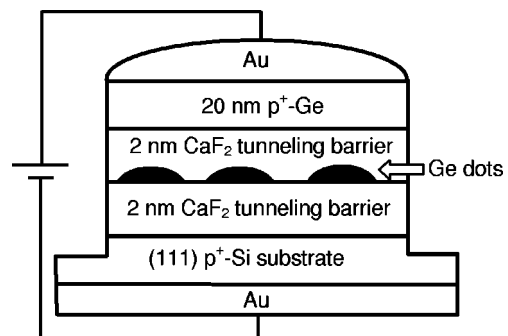


FIG. 1. Schematic of the SET device structure with self-assembled Ge quantum dots.

^{a)}Electronic mail: yakimov@isp.nsc.ru

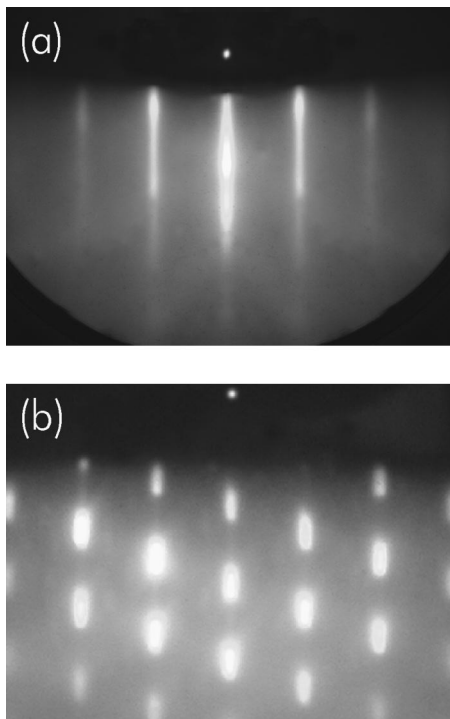


FIG. 2. RHEED patterns after deposition of (a) 2 nm and (b) 3-nm-thick Ge layer on $\text{CaF}_2/\text{Si}(111)$. Azimuth of e -beam incidence is (110) .

cleaning, the silicon substrates were loaded into the growth chamber and heated at 830°C during 20 min in ultrahigh vacuum. A well-defined (7×7) pattern of RHEED was observed after the treatment. The fluorite and Ge were evaporated from molecular cells with a graphite crucible for CaF_2 and with a pyrolytic boron nitride crucible for Ge. Due to molecular mode of CaF_2 sublimation, the stoichiometry of the grown layers was kept naturally. The growth rate of CaF_2 and Ge layers was about 1 nm/min.

First, a bottom 2-nm-thick CaF_2 layer was grown at a substrate temperature of 520°C . When thickness of the fluorite increased up to 1 ML, a reconstruction (7×7) transformed to (1×1) on the RHEED pattern. To avoid faults in the surface structure analysis due to desintegration of the CaF_2 under the e -beam action: (i) examination of the surface structure was made as fast as possible, and (ii) the specimen has being relocated each time after the RHEED pattern was taken. After deposition of the first CaF_2 layer, the sample was annealed at $700\text{--}750^\circ\text{C}$ for 15 min to suppress the leakage current and increase electrical resistivity of the fluorite film. After heating, the RHEED pattern displayed the fractional strikes of $1/3$ order between basic reflexes.

At the second stage, the temperature of the substrate was reduced to $T_s = 490^\circ\text{C}$ for sample No. 120 and to $T_s = 430^\circ\text{C}$ for sample No. 131. Then, the Ge molecular beam was supplied to the surface of specimen. The $1/3$ order strikes on the RHEED pattern disappeared immediately after the Ge layer began to grow. Spontaneous formation of Stranski–Krastanov Ge islands follows by abrupt transformation of the RHEED pattern. Namely, when thickness of Ge layer exceeds 3 nm, the elongated first order strikes transform to the grid of bright spots (Fig. 2). Since reducing T_s results in decreasing of the size of Ge dots, one expects the

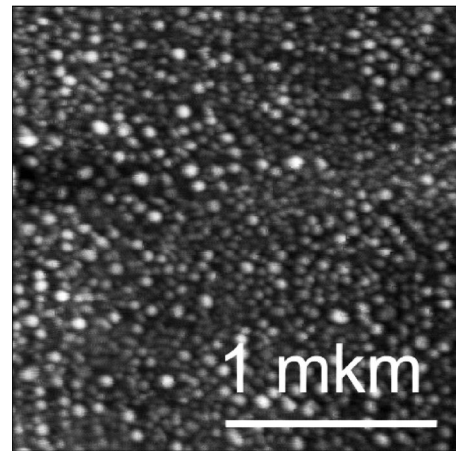


FIG. 3. Two-dimensional AFM image of the Ge islands grown on $\text{CaF}_2/\text{Si}(111)$ at 520°C with the Ge deposition amount of 3 nm.

smaller Ge nanoclusters in sample No. 131 than those in sample No. 120. Because of too small sizes of Ge dots grown under the above conditions, we were not able to observe a reliable image of Ge nanoclusters. However, a clear AFM image of Ge islands can be obtained when the growth temperature is raised up to 520°C and the Ge nanoclusters become as large as 50 nm in diameter (Fig. 3).

A top 2-nm-thick CaF_2 layer was grown above the Ge layer after formation of Ge islands and then annealed at 750°C for 15 min as it has been made for the bottom fluorite layer. The fluorite growth temperature is equal to the growth temperature of Ge in both samples. The finally deposited p^+ -Ge cap layer was selectively etched using the plasma processing and the gold as an etch mask to form the mesas. The active device region is 0.5 mm^2 . The differential transversal conductance $G = dI/dV$ was measured using a two-probe standard lock-in technique at a modulation amplitude $\sim 1 \text{ mV}$ and a frequency of 15 Hz.

The tunneling current derivative as a function of bias voltage at room temperature is shown in Fig. 4. A zero current region and quasiperiodic conductance oscillations with period $\Delta V \approx 100 \text{ meV}$ for sample No. 131 and 80 meV for sample No. 120 accompanied by a negative differential conductance (NDR) are observed for both dot samples. The oscillation structure is completely reproducible for multiple

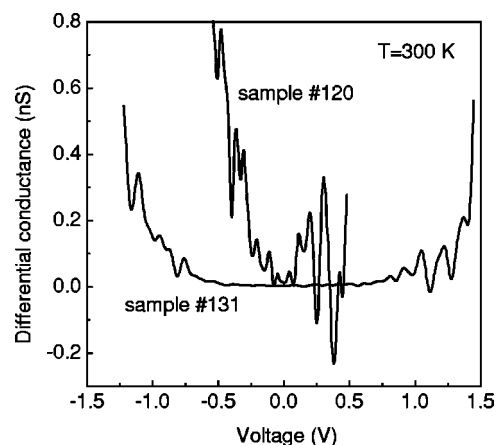


FIG. 4. Conductance–voltage characteristics at $T = 300 \text{ K}$ for two SET devices with Ge quantum dots of different sizes.

scans and not observed in similar samples containing no Ge dots. Since NDR is an inherent feature of resonant tunneling, we attribute the observed conductance oscillations rather to hole tunneling through single-particle energy states in Ge nanoclusters than to single-hole charging. Actually, charging effects are important in tunneling experiments when a carrier (electron or hole) is substantially delayed in the dot during transport. This is possible for strong asymmetric junctions, in which the transmission coefficient through the second barrier (thicker source) is much smaller than that through the first barrier (thinner drain).¹³ Obviously this is not the case in our tunneling devices as both CaF_2 barriers have equal thicknesses.

For symmetric structure, the conductance should show peaks at voltage equal to twice the energies of the bound hole states. From the period of oscillations, we estimate the energy level separation of about 50 meV for small-dot sample No. 131 and of about 40 meV for large-dot sample No. 120. This observation is consistent with the fact that the effect of three-dimensional carrier confinement should weaken with increasing the quantum dot size. In Ref. 14, the separation of the energy levels in Ge self-assembled QDs in silicon matrix was calculated to be 40–50 meV for (10–15)-nm-Ge nanoclusters, which agrees well with the expected size of Ge dots grown at low temperatures.¹¹

In summary, we propose that $\text{CaF}_2/\text{Ge}/\text{CaF}_2/\text{Si}(111)$ heterostructures with self-assembled Ge quantum dots can be

used as the basis of a resonant tunneling diode operating at room temperature. Further work is in progress to reduce size of Ge nanoclusters and to improve device characteristics.

The authors would like to thank Shhamirjan D. G. for assistance. This work has been supported by INTAS (Grant No. 97-10528), RFBR (Grant Nos. 00-02-17900, 00-02-17885) and RFBR-GFEN (Grant No. 99-02-39051).

¹Q. Ye, R. Tsu, and E. H. Nicollan, *Phys. Rev. B* **44**, 1806 (1991).

²E. H. Nicollan and R. Tsu, *J. Appl. Phys.* **74**, 4020 (1993).

³D. W. Boeringer and R. Tsu, *Phys. Rev. B* **51**, 13337 (1995).

⁴M. Fukuda, K. Nakagawa, S. Miyazaki, and M. Hirose, *Appl. Phys. Lett.* **70**, 2291 (1997).

⁵A. Dutta, M. Kimura, Y. Honda, M. Otobe, A. Itoh, and S. Oda, *Jpn. J. Appl. Phys., Part 1* **36**, 4038 (1997).

⁶K. Kim, *Phys. Rev. B* **57**, 13072 (1998).

⁷T. Baron, P. Gentile, N. Magnea, and P. Mur, *Appl. Phys. Lett.* **79**, 1175 (2001).

⁸Y. Inoue and A. Tanaka, *J. Appl. Phys.* **86**, 3199 (1999).

⁹D. M. Pooley, H. Ahmed, H. Mizuta, and K. Nakazato, *J. Appl. Phys.* **90**, 4772 (2001).

¹⁰A. I. Yakimov, V. A. Markov, A. V. Dvurechenskii, and O. P. Pchelyakov, *Philos. Mag. B* **65**, 701 (1992).

¹¹A. I. Yakimov, V. A. Markov, A. V. Dvurechenskii, and O. P. Pchelyakov, *J. Phys.: Condens. Matter* **6**, 2573 (1994).

¹²O. G. Schmidt, U. Denker, K. Eberl, O. Kienzle, F. Ernst, and R. J. Haug, *Appl. Phys. Lett.* **77**, 4341 (2000).

¹³U. Meirav and E. B. Foxman, *Semicond. Sci. Technol.* **10**, 255 (1995).

¹⁴A. V. Dvurechenskii, A. V. Nenashev, and A. I. Yakimov, *Nanotechnology* **13**, 75 (2002).