Ge/Si quantum-dot metal–oxide–semiconductor field-effect transistor

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We report on the operation of Si metal–oxide–semiconductor field-effect transistor with an array of $\sim 10^3$ 10 nm diameter Ge self-assembled quantum dots embedded into the active channel. The drain current versus gate voltage characteristics show oscillations caused by Coulomb interaction of holes in the fourfold-degenerate excited state of the dots at $T \leqslant 200$ K. A dot charging energy of ~ 43 meV (i.e., $> kT = 26$ meV at $T = 300$ K) and disorder energy of ~ 20 meV are determined from the oscillation period and the temperature dependence study of current maxima, respectively. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1488688]

Epitaxial growth of highly strained semiconductors in the Stranski–Krastanov growth mode enables *in situ* fabrication of arrays of 10 nm scale quantum dots [so called self-assembled quantum dots (SAQDs)]. Electronic and optoelectronic nanodevices implemented on Ge self-assembled quantum dots in Si matrix have attracted much attention due to their compatibility with modern Si-based complementary metal–oxide–semiconductor circuitry. This would offer a substantial reduction in complexity and cost of future high performance electronics. Despite the large effort to study the fundamental properties of Ge/Si SAQDs, there are only several attempts of incorporating Ge/Si islands as an active element of semiconductor devices, such as infrared photodetectors,[1–5] and light-emitting[6,7] and resonant-tunneling diodes.[8] Little work has been done on the Ge/Si quantum-dot field-effect transistors (QDFETs), which utilize the quantum transport through discrete energy states in zero-dimensional systems. To date, most work in the field of QDFETs has concentrated on InAs/GaAs SAQDs[9–11] and on Si-based quantum dots (QDs) defined by very sophisticated patterning techniques, such as electron-beam lithography in combination with anisotropic etching[12–15] and selective oxidation,[16,17] or by tunable gates.[18]

In order to raise the operation temperature of QDFETs up to 300 K, the size of QDs has to be smaller than 10 nm. This requirement considerably restricts the possibility of using the lithographic processes for fabrication ultrasmall QDs. In this way the Ge/Si SAQDs, which are formed without an additional lithography procedure and whose diameter can be achieved as small as ~ 10 nm,[2] are more advantageous and, hence, more relevant for application in QDFETs operating at room temperature.

Previously, we demonstrated a QDFET with an array of 3×10^7 Ge SAQDs embedded into the active channel of a Si metal–oxide–semiconductor field-effect transistor (MOSFET).[19] The device was fabricated on a silicon-on-insulator (SOI) substrate prepared by the separation by implanted oxygen technique. The channel was a Si island of 100 μm width and 108 μm length which rests on SiO_2. The area of the MOSFET gate was 100×100 μm^2. However, clear drain current oscillations with a gate voltage due to successive loading of holes into the dots were not observed. The reasons are (i) the leakage current across the Si layer leading to the large background varying with the voltage, and (ii) significant broadening of the current peaks due to statistical fluctuations of the dot sizes and Coulomb potentials from randomly distributed charged QDs in the dot ensemble. These drawbacks are eliminated in this letter. First, the drain current leakage is reduced by reducing the superficial Si layer thickness in a SOI substrate. Second, the average Ge SAQDs lateral dimensions are decreased from 15 (Ref. 19) to 10 nm. The stronger carrier confinement in the dots provides the larger energy level separation resulting in a more clear resolution of the current peaks at high temperatures. Third, inhomogeneous broadening due to long-range dot size variations and random Coulomb potentials are reduced by decreasing the QDFET size from 100 to ~ 1 μm and by using the gate recess configuration.[10]

The starting material was a SOI (001) substrate with a 150-nm-thick p-type superficial Si film. First, the SOI layer was thinned to 47 nm by thermal oxidation. After removing SiO_2, a 20-nm-thick undoped Si buffer layer was grown at 800 °C by molecular beam epitaxy. Next, the Ge self-assembled dots were grown at 300 °C with nominal thickness of eight monolayers and subsequently embedded in 20 nm of Si. The average in-plane diameter and height of the Ge dots are 10 and 1 nm, respectively. The density of the dots is 4×10^{11} cm^{-2}. To supply holes on the dots, a boron delta-doping (6×10^{12} cm^{-2}) Si layer inserted 20 nm above the Ge layer was grown. A 30-nm-thick undoped Si cap layer was then deposited at 500 °C. The channel was patterned by photolithography to form a Si island of 4 μm length and 1 μm width, etched down to the underlying SiO_2. Source and drain electrodes were made using Al evaporation and annealing at 450 °C in a N_2 atmosphere. A plasma-enhanced chemical-vapor deposition silicon dioxide of 60 nm thickness was deposited as the gate insulator and, finally, a Al gate of 4 μm width and 1 μm length was formed. The amount of oxide charge, estimated from the admittance measurements, was about 3×10^{10} cm^{-2}. Figure 1 shows an atomic force microscopy picture of the transistor. Several samples with

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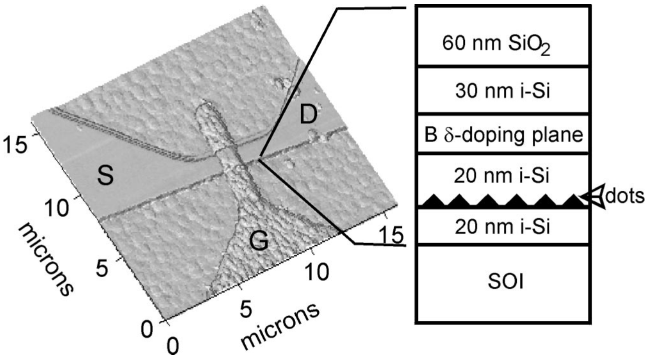

FIG. 1. Atomic force microscopy image and schematic cross section of the transistor channel. The source, drain, and the gate are labeled by S, D, and G, respectively.

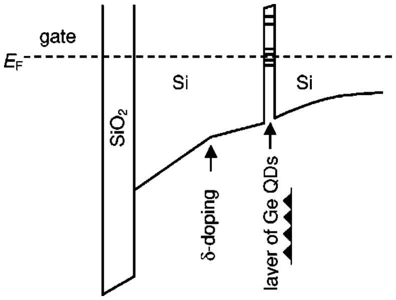

FIG. 3. Top of the valence band of the transistor for positive gate bias. The SOI substrate is not shown. The holes reside in the Ge dots. When the Fermi level is aligned with the quantum levels in the Ge dots at a certain gate voltage, holes will flow through that quantum level in the plane of Ge SAQDs.

designed channel widths W ranging from 2 to 1 μm are fabricated. The sidewall depletion width is determined to be 0.9 μm from measurements of drain current versus W at zero gate voltage. Assuming a uniform density of 4000 dots per μm^2 the different gate areas of the samples contain a number of active dots from 400 to 4000.

The hole concentration in the boron δ-doping Si layer is sufficient to fill, after spatial transfer, all hole bound states in the Ge islands and to populate two-dimensional states in the Ge wetting layer. As a result, the channel conductance at zero gate voltage is found to show the nonactivated behavior and depend only slightly on temperature.

The drain current (I_d) as a function of the gate voltage (V_g) was measured at different temperatures with the drain voltage fixed at 5 mV. Figure 2 shows the typical $I_d - V_g$ characteristics of the 1 μm gate QD transistor. When a positive bias is applied to the gate the channel is depleted and current flow between the source and drain contacts is suppressed. Above the threshold voltage $V_{\text{th}} \simeq 4$ V the deep hole states in the dots come into resonance with the Fermi energy and the current starts to oscillate (Fig. 3).

At room temperature, the current bump is clearly observable around 6 V. As the temperature decreases, four well-pronounced equidistant peaks with a gate voltage separation $\Delta V_g \simeq 1.1$ V appear after the onset of the conductance. The number and relative position of the peaks are well reproducible at different cold cycles and in different samples of similar sizes. Thus, we can omit mesoscopic conductance fluctuations[20] as a possible mechanism of the current oscillations. It follows from our previous investigations of the field effect, admittance, and capacitance spectra in Si modulation-doped structures with similar Ge quantum dots[19,21,22] that when we leave the continuum and enter the tunneling regime with increasing gate bias, we would expect four equidistant current peaks (tunneling through fourfold-degenerate excited state in the Ge QDs), then a voltage (energy) gap, and two additional peaks corresponding to transport through the twofold-degenerate hole ground state (Fig. 3). Since we only observe four maxima right above the transport continuum, we relate these peaks to hole transport through the excited state of Ge/Si SAQDs. A very similar fine-structure consistent with four maxima, separated by the Coulomb blockade energy E_C, has been observed recently by Schmidt *et al.*[11] in InAs/GaAs QDFETs. We may ask why we do not observe current maxima associated with a filling of the hole ground state. Due to confinement and Coulomb effect, the energy difference between loading the second hole into the ground state and the first hole into the excited state of the 8 ML Ge SAQDs is approximately 200 meV.[22] Simple estimates using the gate modulation coefficient (determined later) yield that filling of the ground state is expected to be at $V_g \approx 16$ V but, in this region, large leakage current through the gate insulator prevents measurements of $I_d - V_g$ characteristics.

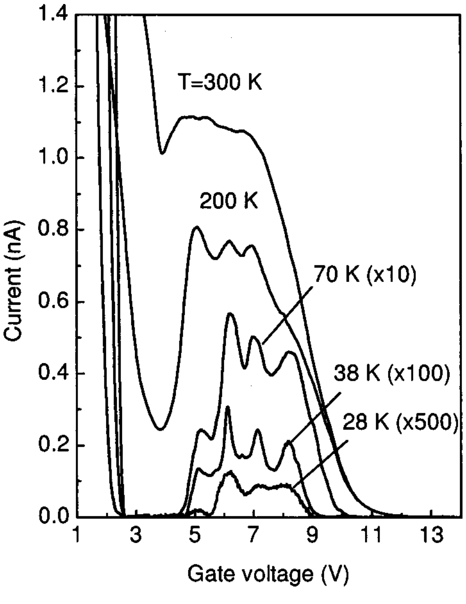

FIG. 2. Gate voltage dependence of drain current at various temperatures.

The charging energy (E_C) of the dots can be determined by using $E_C = \eta e \Delta V_g$, where the gate modulation coefficient η relates the gate voltage to the hole energy inside the dots. This coefficient can be calculated from the temperature dependence of the full width at half maximum (FWHM) of the current peaks, which, for a single dot showing Coulomb blockade oscillations, should be broadening with T as $3.5 k_B T/(\eta e)$,[23] where k_B is Boltzmann's constant. By measuring the FWHM averaged over four peaks as a function of temperature (Fig. 4), we obtain $\eta = (3.9 \pm 0.3) \times 10^{-2}$, with a residual FWHM $V_0 = 0.49 \pm 0.05$ V which is a result of statistical fluctuations in the dot ensemble. Based on this calculation, the estimated charging energy is 43 ± 3 meV.

In Fig. 4, we depict the temperature dependence of the current maxima. A clear thermally enhanced transport

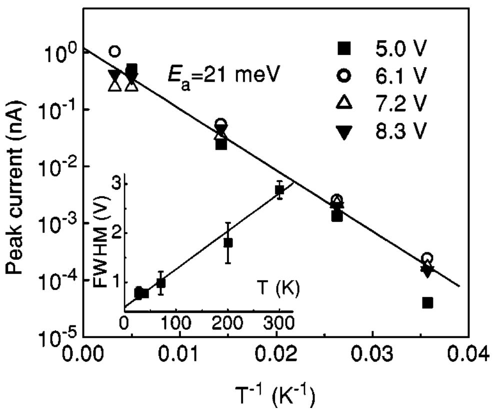

FIG. 4. Temperature dependence of the current maxima at different gate voltages. Inset: Temperature dependence of the average FWHM of four current maxima with a linear fit to the data. To obtain the FWHM of each peak, the observed current oscillations were decomposed into four Gaussians.

through the dots with the activation energy $E_a = 21 \pm 3$ meV is evident. Several scenarios could lead to such a behavior, such as thermal activation of holes from the dots over the barriers[24] and hole tunneling between neighboring dots.[25] In a latter case, the activation energy is a typical disorder energy in the system, which comes from dispersion of the dot sizes and potential fluctuations caused by random distribution of the charged dots and interface states. Since the experimental value E_a is the same for all peaks, i.e., it does not depend on the effective barrier height, we attribute the conduction mechanism to the nearest-neighbor hopping of holes between the dots. With scanning the gate voltage the Fermi level moves across the zero-dimensional density of states. The maximum current occurs when the given hole level in the dots is half-filled, as this maximizes the product of possible initial and final states for tunneling process and avoids increasing the energy of the system due to appearance of extra charge in a final dot.

The disorder energy, E_d, in ensemble of the dots can be found from residual FWHM using $E_d = \eta e V_0$. For $V_0 = 0.49 \pm 0.05$ V and $\eta = (3.9 \pm 0.3) \times 10^{-2}$, we obtain $E_d = 19 \pm 3$ meV, which is consistent with the experimental value of activation energy observed in Fig. 4.

In summary, we have demonstrated Ge/Si quantum-dot metal–oxide–semiconductor field-effect transistor with the active channel containing $\sim 10^3$ Ge self-assembled islands. The drain current shows Coulomb blockade oscillations at temperatures as high as 200 K. The charge-transfer mechanism in the transistor channel is identified as being due to nearest-neighbor hopping of holes between the Ge dots with the typical hopping energy determined by disorder in the quantum dot ensemble. Further work is in progress to reduce the number of dots in the channel.

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